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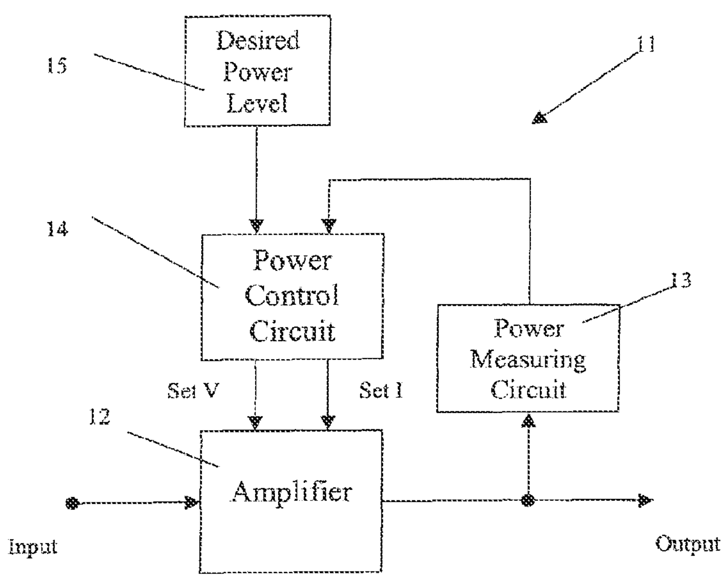
(54) Title: AMPLIFIER CIRCUIT



(57) Abstract: An amplifier circuit (11) comprises an amplifier (12), an indicator of desired power (15), a power control circuit (14) and a power measuring circuit (13). The amplifier (12) amplifies an input signal to produce an output signal, and has an input for controlling a supply current (I) and an input for receiving a supply voltage (V) and supply current (I), for driving the amplifier. The power control circuit calculates and applies values for both a supply voltage (V) and a supply current (I), according to any one of a plurality of desired power levels, in order to operate the amplifier with maximum efficiency over a wide range of power levels. The power control circuit may further comprise a power control loop whereby adjustment of the output power can also be effected according to a measurement of output power and a desired level of output power.

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AMPLIFIER CIRCUIT

The invention relates to an amplifier circuit and a method of operating an amplifier.

Background of the Invention

Electronic amplifiers, and in particular power amplifiers, are widely used in audio equipment and in the transmitters of telecommunication transceivers. One of the requirements for such amplifiers is to obtain the best possible efficiency. For the purpose of this description, amplifier efficiency can be regarded as the ratio between alternating-current (AC) output power and direct-current (DC) input power supplied to the amplifier.

In known amplifiers, this requirement is addressed by first specifying the required output power level, and then optimising the amplifier for that specific output power level. One known way of optimising the amplifier is to select an optimum load for the required output power level. Another is to employ a switchable load that can be adjusted according to different required output power levels. Usually, the output power level, in the case of a single value of load, is specified to be either the highest operating level, or slightly below the highest operating level in order to minimise the effect of reduced efficiency, measured as lost dissipated power, at higher power levels for which dissipated loss is greatest.

However, a problem of this approach is that it is only possible, for a given load, to maintain near-optimum efficiency for the specified output

power level for that load. If an amplifier optimised for a specified output power level is used for a different power level, then a significant reduction in efficiency results if the amplifier is not re-adjusted (e.g. by adjusting the load). For example, if a class-A amplifier with a fixed supply voltage is optimised for an output power level of P Watts, then the amplifier, when operated at that output power level P, will have an efficiency that approaches the ideal 50% (the theoretical maximum for a transistor saturation voltage V_{sat} of zero). If the same class-A amplifier is operated at an output power level of P/2 Watts, then the theoretical best obtainable efficiency is 25%.

The invention aims to provide an amplifier whose efficiency can be optimised for a range of output power levels.

Summary of the Invention

According to one aspect of the invention, there is provided an amplifier circuit comprising: an amplifier for amplifying an input signal to produce an output signal, the amplifier being supplied by a supply voltage and a supply current ; and control means for adjusting, in accordance with a transfer function, both the supply current and supply voltage in order to optimise amplifier efficiency.

According to another aspect of the invention, there is provided an amplifier circuit comprising:an amplifier for amplifying an input signal to produce an output signal, the amplifier having a current-control signal input for determining a supply current and an input for receiving both a supply

voltage V and supply current I for driving the amplifier; means for specifying a desired power level; and control means for calculating values of supply current I and supply voltage V in order to optimise amplifier efficiency at the specified power level, and for applying the corresponding current-control signal and a corresponding supply voltage to the respective inputs of the amplifier.

The control means may be operable to adjust the supply current I and the supply voltage V to maximise the amplifier efficiency in accordance with the variable desired output power level P, and to substantially maintain constant the amplifier efficiency over a range of amplifier output power levels P.

In practice, the amplifier circuit may comprise a transistor, and the control means may be operable to adjust the supply voltage V such that

$$V = \sqrt{2RP} + V_{sat},$$

wherein R is a real impedance presented at an output of the transistor die, and V_{sat} is the transistor saturation voltage. The supply current I is adjusted to

$$I = \frac{V}{R}.$$

Thereby, the amplifier efficiency can be the same (i.e. near-ideal) for a wide range of output power levels. This is particularly advantageous for equipment that is required to operate at more than one output power level. This is achieved without requiring re-adjustment of the load impedance. In other words, a constant value of load impedance may be used for different output power levels without impairing the amplifier efficiency.

A typical application for the amplifier circuit would be for dynamic power control in a base station (terrestrial or satellite) of a telecommunications system, or indeed in a mobile terminal where efficiency is a key parameter and where the output signal power level can vary dynamically over time and over a wide range of levels.

Also, if a battery is used for supplying power to the amplifier, by adjusting the voltage V input to the amplifier, rather than supplying the amplifier direct from the battery, the amplifier's efficiency is independent of a change of charge in the battery, e.g. as a result of battery discharge. A DC-to-DC converter could be used to provide the variable supply voltage. DC-to-DC converters have relatively high efficiency.

Furthermore, by adjusting both the input supply voltage and the supply current, the levels of generated harmonics in the case of non-class-A operation can be controlled more easily. That is, a symmetrical waveform can be produced for a wide range of output power levels, with voltage limiting and current limiting occurring at both peaks and troughs of the signal waveform. This reduces the level of second harmonic generated.

According to a further aspect of the invention, there is provided a method of operating an amplifier for amplifying an input signal to produce an output signal, the method comprising: supplying the amplifier with a supply voltage and a supply current; and adjusting, in accordance with a transfer function, both the supply current I and supply voltage V in order to optimise amplifier efficiency.

The above and further features of the invention are set forth with particularity in the appended claims and together with advantages thereof will become clearer from consideration of the following detailed description of an exemplary embodiment of the invention given with reference to the accompanying drawings.

Brief Description of the Drawings

In the drawings:

Figure 1 illustrates a transistor amplifier circuit;

Figure 2 illustrates collector characteristic curves and a dynamic load line of the transistor of Figure 1;

Figure 3 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and $½I_s$;

Figure 4 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and I_s;

Figure 5 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and $2I_s$;

Figure 6 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at $1.5V_s$ and $1.5I_s$;

Figure 7 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at $0.75V_s$ and $0.75I_s$;

Figure 8 is a flow diagram of one method of optimising the efficiency of an amplifier;

Figure 9 is a flow diagram of another method of optimising the efficiency of an amplifier;

Figure 10 is an outline block diagram showing the overall function of the amplifier circuit;

Figure 11 is a more detailed block diagram of the amplifier circuit; and

Figure 12 is another detailed block diagram of the amplifier circuit.

Detailed Description of an Embodiment of the Invention

Referring to Figure 1 of the accompanying drawings, there is shown an amplifier 1 comprising a NPN bipolar transistor TR1. An inductor L1 is connected to a collector terminal 2 of the transistor TR1. Likewise, an inductor L2 is connected to a base terminal 3 of the transistor TR1. A load Z_{load} is connected to the collector terminal 2 via a lossless matching circuit M1. The lossless matching circuit transforms the load Z_{load} into a completely real impedance R_{opt}. Accordingly, the effective load presented to the transistor collector is R_{opt}. Preferably, the matching circuit M1 includes any transistor parasitics (collector-emitter capacitance and load inductance) so that R_{opt} is the impedance presented to the transistor die. R_{opt} is called the dynamic load impedance and has the value of a pure resistance, measured in units of Ohms.

Referring now to Figure 2, there are shown the collector characteristic curves (1) of the transistor TR1 together with dynamic load line (2). The horizontal axis of the graph corresponds to the collector-emitter voltage V_{ce}.

(If, in the alternative, a field-effect transistor (FET) was used instead of the NPN bipolar transistor TR1, V_{ce} would correspond to the drain-source voltage V_{ds} (with the source at zero volts)). The vertical axis of the graph corresponds to the collector current I_{cc} (the equivalent for a FET would be the drain current I_{dd}). The multiple curves (1) correspond to different values of base current (corresponding to different values of gate voltage for a FET). The gradient of the dynamic load line is equal to $-(1/R_{opt})$. V_s designates a particular value of DC supply voltage on the collector, while I_s designates a particular value of the DC collector supply current.

In Figure 2, the collector AC voltage is a sine wave of amplitude V_s, and the collector AC current is a sine wave of amplitude I_s. For the transistor TR1 to demonstrate the characteristics of Figure 2, it is biased to obtain maximum efficiency. The condition for maximum efficiency is represented by load line (2) and corresponds to a unique value of R_{opt}. That is, R_{opt} is predetermined such that, as the output power level is increased from zero, eventually, when limiting starts to occur, both voltage and current limiting begin simultaneously.

The output power level is equal to

$$P_{ac} = \frac{(V_{ce} - V_{sat})^2}{2R_{opt}} \qquad \text{(equation 1),}$$

where P_{ac} is in units of Watts, V_{ce} and V_{sat} are in units of Volts, and R_{opt} is in units of Ohms. In Figure 2, $V_{ce} = V_s$. Thus

$$P_{ac} = \frac{(V_s - V_{sat})^2}{2R_{opt}} \qquad \text{(equation 2).}$$

As V_{sat} tends to zero, and the DC collector supply current $I_s = \frac{V_s}{R_{opt}}$, P_{ac} tend to

$$P_{ac} \approx \frac{V_s^2}{R_{opt}} = \frac{V_s \cdot I_s}{2} \qquad \text{(equation 3).}$$

Since the DC input power is $V_s \cdot I_s$, the resulting theoretical efficiency (as V_{sat} approaches zero) is 50%.

Equation 2 can be used to calculate the optimum DC supply voltage V_s:

$$V_s = \sqrt{2R_{opt}P_{ac}} + V_{sat} \qquad \text{(equation 4).}$$

From V_s, the required DC collector supply current, I_{cc}, can be calculated:

$$I_{cc} = \frac{V_s}{R_{opt}} \qquad \text{(equation 5).}$$

Figures 3, 4 and 5 illustrate three graphs of collector characteristic curves and dynamic load lines. In each of these graphs, $V_{ce} = V_s$ is a constant value, and the load line gradient, derived from R_{opt}, is constant ($-\frac{1}{R_{opt}}$). For each graph, the value of collector DC supply current I_{cc} is different (a multiple or sub-multiple of I_s). For simplification, the characteristic curves have been approximated such that V_{sat} is zero. The locus of collector voltage V_{ce} and the collector current I_{cc} is the load line.

Figure 3 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and $\frac{1}{2}I_s$ where V_s and I_s are

constants. In Figure 3, $I_{cc} = \frac{I_s}{2}$. For the limiting case where the signal is maximum for linear operation (where limiting is just about to occur), the efficiency is 25%.

Figure 4 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and I_s. In Figure 4, $I_{cc} = I_s$ to bias the transistor to obtain maximum efficiency. The collector AC voltage is a sine wave of amplitude V_s and the collector current is a sine wave of amplitude I_s. This corresponds to the conditions of Figure 2, subject to V_{sat} being assumed zero. In this condition, the amplifier is on the threshold limit of saturation, where the maximum voltage and current swing are obtained whilst maintaining linear (class A) operation with no limiting of either voltage or current. Thus, the theoretical efficiency is 50%.

Figure 5 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at V_s and $2I_s$. In Figure 5, $I_{cc} = 2I_s$. It can be seen that, as the signal amplitude is increased from zero, voltage limiting will occur first on the voltage minima, but not on the voltage maxima, giving rise to a high level of second harmonic relative to the fundamental. If, for the supply current of Figure 5, the amplifier is operated at maximum power level whilst maintaining linear (class A) operation (as shown), then the efficiency is 25%.

Figures 6 and 7 illustrate two examples where both the supply voltage and the supply current Icc are adjusted simultaneously to give a theoretic efficiency of 50% for each of two different power levels. Figure 6 illustrates

idealised collector characteristic curves and a dynamic load line with a DC operating point at 1.5Vs and 1.5Is. Figure 7 illustrates idealised collector characteristic curves and a dynamic load line with a DC operating point at $0.75V_s$ and $0.75I_s$.

Figures 8 and 9 illustrate slightly different ways in which the amplifier may be controlled. Figure 8 is a flow diagram of one method of optimising the efficiency of an amplifier. In Figure 8 a required level of the power in the output from the amplifier is accepted at stage 3. Next, at stage 4, a value for the supply voltage V is calculated followed by a calculation 5 of the current I. The calculated voltage and current are then applied 6 to the amplifier to optimise its efficiency. Figure 9 is a flow diagram of another method of optimising the efficiency of an amplifier. In Figure 9 the same operations are performed, but the voltage and current calculations of stages 4 and 5 are calculated simultaneously or non-sequentially.

Figure 10 of the accompanying drawings is a schematic circuit diagram of an amplifier circuit 11 with supply current and supply voltage control. The amplifier circuit 11 comprises an amplifier 12, which may for example comprise the amplifier of Figure 1. The amplifier 12 has a current-control signal input ($I_{control}$) for determining a supply current I and an input for receiving both a supply voltage V and supply current I, for driving the amplifier. The $I_{control}$ signal operates, in the case of a bipolar transistor amplifier, to adjust the base bias current of the transistor, and this in turn acts to adjust the supply current (collector current). In the case of a FET amplifier,

the $I_{control}$ signal operates to adjust the gate voltage of the transistor, which in turn acts to adjust the supply current (drain current).

The amplifier 12 receives a signal on an input line and outputs an amplified version of the received signal on an output line. A power measuring circuit 13, which may be an envelope detector for example, is connected to the output line and measures power in the signal thereon. It will be appreciated that a power measuring circuit could instead be placed in series with the output line, but would nevertheless perform the same power measuring function.

A signal representing power is supplied from the power measuring circuit 13 to a power control circuit 14. The power control circuit 14 also receives a desired power level signal from a desired power level indicator 15. In an audio amplifier circuit, the desired power level indicator could be a variable resistor connected to a volume control knob for selection by a user. In cellular phone systems power control is used to control the power output by a cellular telephone. The power control essentially comes from one or both of two sources, namely from the cellular telephone itself or from the cellular system. In the former case power control is effected by measuring power in communication signals received by the cellular telephone and adjusting the output power in inverse proportion thereto. In the latter case power control is effected in the form of command signals from a mobile controller in the cellular system, which controller measures power in signals received from the cellular telephone and sends command to the cellular telephone to adjust its

output power in order to meet desired parameters within the system. Thus, in an amplifier for a cellular telephone, the desired power level indicator could be a register that receives data from a source internal or external to the cellular telephone.

The power control circuit uses the desired power level signal to calculate and generate the above discussed supply voltage V and supply current I. The power control circuit 14 also uses the desired power level signal from desired power level indicator 15 together with the output power signal from the power measuring circuit 13 to adjust further the value of V or I to control accurately the desired output power.

In general terms, efficiency is controlled by adjusting both supply voltage and supply current according to a desired power level, using a transfer function. The transfer function may be realised using a circuit which applies the above-discussed equations or one or more look up tables comprising empirically determined relationships between power levels, supply currents and supply voltages. Either way, the values of supply current I and supply voltage V necessary to achieve optimum amplifier efficiency for the desired/required power output are determined by the power control circuit 14. The power control circuit 14 then adjusts the supply current I and supply voltage V accordingly.

Figure 11 is a more detailed block diagram of the amplifier circuit, and shows how efficiency and power are controlled independently. Power control is achieved by adjusting the supply voltage in accordance with measured

output power. The required power level is input to a calculating unit 17 in the power control circuit 14, which calculates values for V, I, and the corresponding value of $I_{control}$. $I_{control}$ at the calculated value is input to the amplifier 12 at line 19. In this way the efficiency of the amplifier is controlled.

The supply voltage V at the calculated value is output on line 20 to a summing circuit 21. The output from the power measuring circuit 13, i.e. a signal representing actual power, is input to a control unit 22, which also receives the required power level signal from the desired power level register 16. The control unit 22 serves as a comparator that provides a signal proportional to the difference between the required power level signal and the signal representing actual power.

The output of the control unit 22 is also input to the summing circuit 21, which thus adjusts the supply voltage V applied to the amplifier 12 depending on the difference between the desired power and the actual power. The summing circuit 21, the control function 22, the amplifier 12 and the power measuring circuit 13 thus form elements of a control loop to control the output power of the amplifier 12 as a separate parameter, independent of the controlling of efficiency.

Figure 12 is another detailed block diagram of the amplifier circuit, showing an alternative arrangement in which power control is achieved by adjusting the supply current in accordance with measured output power. The arrangement in Figure 12 is similar to that shown in Figure 11, except that the

output power is controlled by adjusting the supply current, as opposed to the supply voltage.

In an alternative arrangement (not shown) the power control circuit 14 additionally or alternatively controls the supply voltage and current of the amplifier circuit 12 in order to optimise the efficiency of the amplifier, based on the input power to the amplifier and the gain of the amplifier. In this arrangement the power measuring circuit 13 would take measurements of the input signal and then adjust the supply voltage and current of the amplifier accordingly. A value could be assumed for the gain of the amplifier based upon knowledge of the characteristics of the amplifier. Alternatively, the gain could be measured by using a second power measuring circuit to measure the output power. Independent accurate power control could be implemented as shown in Figure 11 or Figure 12.

Having thus described the invention by reference to a preferred embodiment it is to be well understood that the embodiment in question is exemplary only and that modifications and variations such as will occur to those possessed of appropriate knowledge and skills may be made without departure from the spirit and scope of the invention as set forth in the appended claims and equivalents thereof.

CLAIMS:

1. An amplifier circuit comprising:

an amplifier for amplifying an input signal to produce an output signal, the amplifier being supplied a supply voltage V and being biased by a bias current I; and

control means for adjusting, in accordance with a transfer function, both the bias current I and supply voltage V in order to optimise amplifier efficiency.

2. An amplifier circuit as claimed in claim 1, further comprising means for specifying a desired output power, and wherein the transfer function serves to calculate values for both the bias current I and supply voltage V depending on the desired output power.

3. An amplifier circuit as claimed in claim 1 or 2, wherein in use the output signal is output to a load impedance, and the transfer function serves to calculate values for both the bias current I and supply voltage V depending on the load impedance.

4. An amplifier circuit as claimed in any preceding claim, wherein the control means comprises a power measuring circuit for measuring power in the signal output from the amplifier, and the transfer function serves to

calculate values for at least one of the bias current I and supply voltage V depending on the measured power in the output signal.

5. An amplifier circuit as claimed in claim 4, further comprising means for specifying a desired output power level, and wherein the transfer function serves to calculate values for both the bias current I and supply voltage V depending on the desired power.

6. An amplifier circuit as claimed in any preceding claim, wherein the control means comprises a look up table and the transfer function is calculated by way of the look up table.

7. An amplifier circuit as claimed in any preceding claim, wherein the control means is operable to adjust the bias current I and supply voltage V to maintain substantially constant the amplifier efficiency over a range of amplifier output power levels P.

8. An amplifier circuit as claimed in claim 7, wherein the amplifier output power level P is an AC output power level.

9. An amplifier circuit as claimed in claim 8, wherein the amplifier comprises a transistor, and wherein a real impedance R is presented to an output of the transistor die.

10. An amplifier circuit as claimed in claim 9, wherein the control means is operable to adjust the supply voltage V such that

$$V = \sqrt{2R \cdot P} + V_{sat},$$

wherein V_{sat} is the transistor saturation voltage.

11. An amplifier circuit as claimed in claim 10, wherein the control means is operable to adjust the bias current I such that

$$I = \frac{V}{R}.$$

12. An amplifier circuit as claimed in claim 10, wherein the control means is operable to adjust the bias current I such that

$$I = \sqrt{2(P/R)}$$

13. An amplifier circuit as claimed in claim 10, wherein the control means is operable to adjust the bias current I such that

$$I = (\sqrt{2(P/R)} + V_{sat})/R$$

14. An amplifier circuit as claimed in any of claims 9 to 13, wherein the transistor is a bipolar transistor, and the bias current I is the collector current of the bipolar transistor.

15. An amplifier circuit as claimed in any of claims 9 to 13, wherein the transistor is a field-effect transistor, and the bias current I is the drain current of the field-effect transistor.

16. An amplifier circuit as claimed in any of claims 9 to 15, wherein the load R is predetermined such that when limiting starts to occur on an increase of the amplifier output power level P, both voltage and current limiting start substantially simultaneously.

17. An amplifier circuit as claimed in any preceding claim, wherein the control means is operable to adjust the bias current I and the supply voltage V simultaneously.

18. A mobile terminal for a telecommunications system, the mobile terminal comprising an amplifier circuit as claimed in any preceding claim.

19. A base station for a telecommunications system, the base station comprising the amplifier of any of claims 1 to 17.

20. A telecommunications system comprising one or more mobile terminals according to claim 16, and one or more base stations according to claim 19.

21. The telecommunications system of claim 20, wherein the telecommunications system is a CDMA-based system.

22. A method of operating an amplifier for amplifying an input signal to produce an output signal, the method comprising:

supplying the amplifier with a supply voltage V;

supplying the amplifier with a supply current I; and

adjusting, in accordance with a transfer function, both the supply voltage V and supply current I in order to optimise amplifier efficiency.

23. A method as claimed in claim 22, further comprising specifying a desired output power, and calculating values for both the bias current I and supply voltage V depending on the desired output power.

24. A method as claimed in claim 22 or 23, further comprising outputting an the output signal from the amplifier to a load impedance, and calculating values for one or more of the bias current I and supply voltage V depending on the load impedance.

25. A method as claimed in any of claims 22 to 24, further comprising measuring power in the signal output from the amplifier, and calculating values for both the bias current I and supply voltage V depending on the measured power in the output signal.

26. A method as claimed in claim 25, further comprising specifying a desired output power level, and calculating values for both the bias current I and supply voltage V_s depending on the desired power.

27. A method as claimed in any of claims 22 to 26, further comprising using a look up table to calculate the transfer function.

28. A method as claimed in any of claims 22 to 27, further comprising adjusting the bias current I and supply voltage V to maintain substantially constant the amplifier efficiency over a range of amplifier output power levels P.

29. A method as claimed in claim 28, wherein the amplifier output power level P is an AC output power level.

30. A method as claimed in claim 29, wherein the supply voltage V is adjusted such that

$$V = \sqrt{2R \cdot P} + V_{sat},$$

wherein V_{sat} is the transistor saturation voltage.

31. A method as claimed in claim 30, wherein the bias current I is adjusted such that

$$I = \frac{V}{R}.$$

32. A method as claimed in claim 30, wherein the bias current I is adjusted such that

$$I = \sqrt{2(P/R)}$$

33. A method as claimed in claim 30, wherein the bias current I is adjusted such that

$$I = (\sqrt{2(P/R)} + V_{sat})/R$$

34. A method as claimed in any of claims 30 to 33, wherein the transistor is a bipolar transistor, and the bias current I is the collector current of the bipolar transistor.

35. A method as claimed in any of claims 30 to 33, wherein the transistor is a field-effect transistor, and the bias current I is the drain current of the field-effect transistor.

36. A method as claimed in any of claims 30 to 35, further comprising predetermining the load R, and, on an increase of the amplifier output power level P, limiting substantially simultaneously both voltage and current.

37. A method as claimed in any of claims 22 to 36, further comprising adjusting the bias current I and the supply voltage V substantially simultaneously.

38. An amplifier circuit comprising:

an amplifier for amplifying an input signal to produce an output signal, the amplifier having a current-control signal input for determining a supply current and an input for receiving both a supply voltage V and supply current I for driving the amplifier;

means for specifying a desired power level; and

control means for calculating values of supply current I and supply voltage V in order to optimise amplifier efficiency at the specified power level, and for applying the corresponding current-control signal and a corresponding supply voltage to the respective inputs of the amplifier.

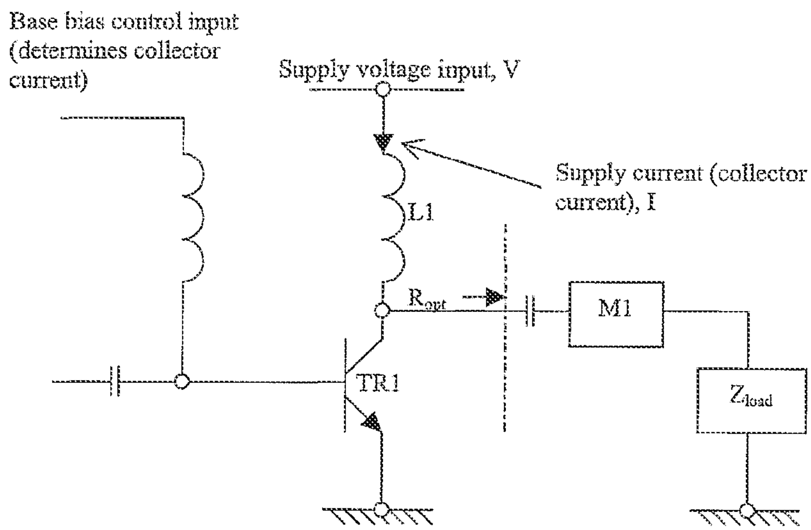
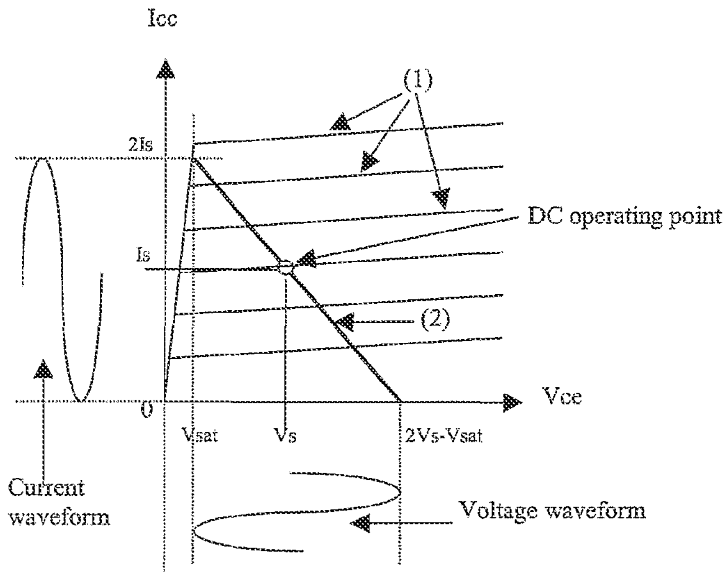

Base bias control input (determines collector current)
Supply voltage input, V
Supply current (collector current), I
L1
R_{opt}
M1
TR1
Z_{load}

FIGURE 1

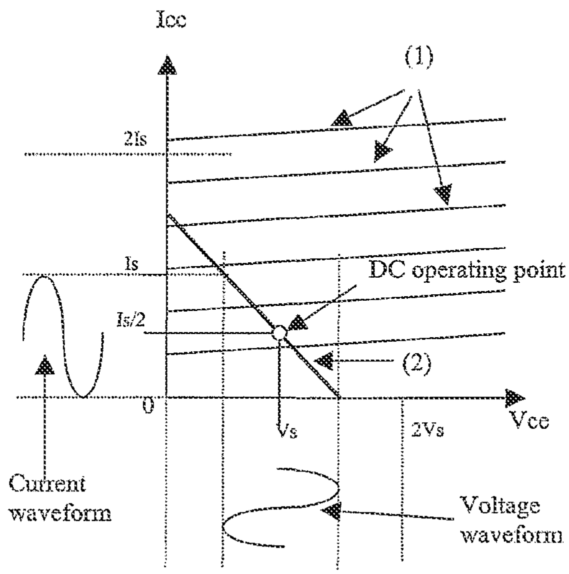


DC power = Vs*Is

AC power = [(Vs-Vsat)*Is]/2

Efficiency ≅ 50% (as Vsat →0)

FIGURE 2

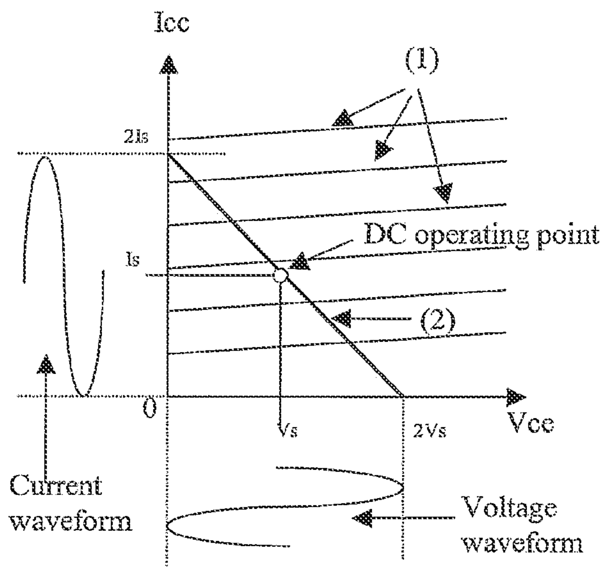


DC power = Vs*Is/2

AC power = (Vs*Is)/8 (Vsat→0)

Efficiency = 25%

FIGURE 3

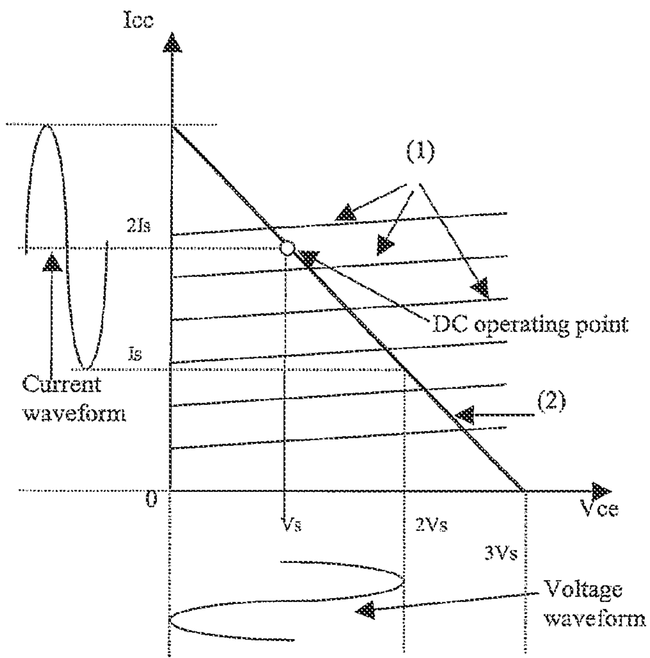


DC power = Vs*Is

AC power = (Vs*Is)/2 (Vsat→0)

Efficiency = 50%

FIGURE 4

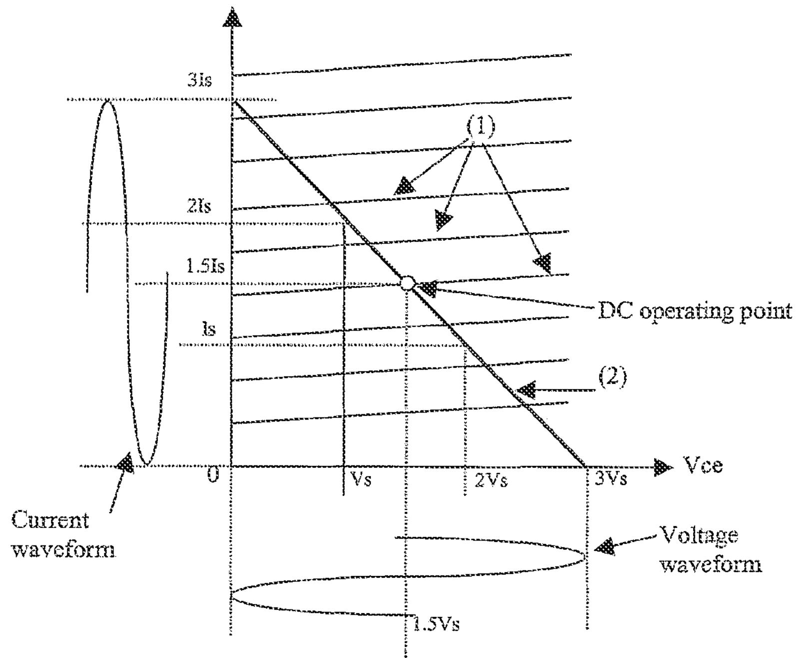


AC power = (Vs*Is)/2 (Vsat→0)

DC power = 2Vs*Is

Efficiency = 25%

FIGURE 5

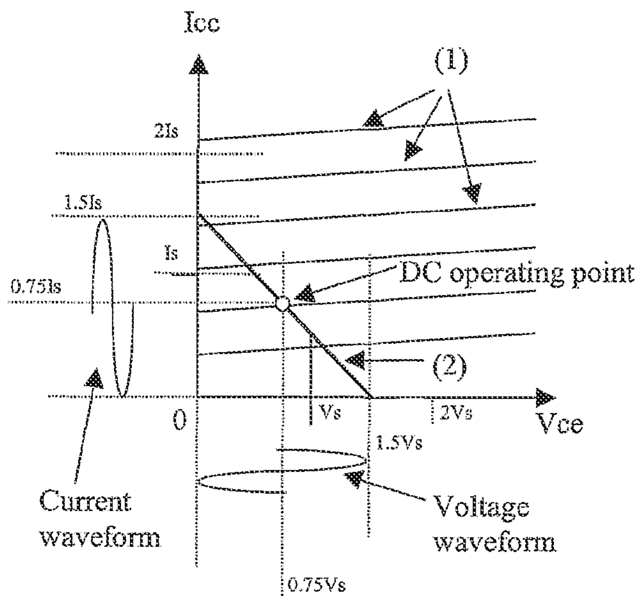


AC power = (1.5Vs*1.5Is) (Vsat→0)

DC power = (1.5Vs*1.5Is)/2

Efficiency = 50%

FIGURE 6



AC power = (0.75Vs*0.75Is)/2
(Vsat→0)

DC power = 0.75Vs*0.75Is

Efficiency = 50%

FIGURE 7

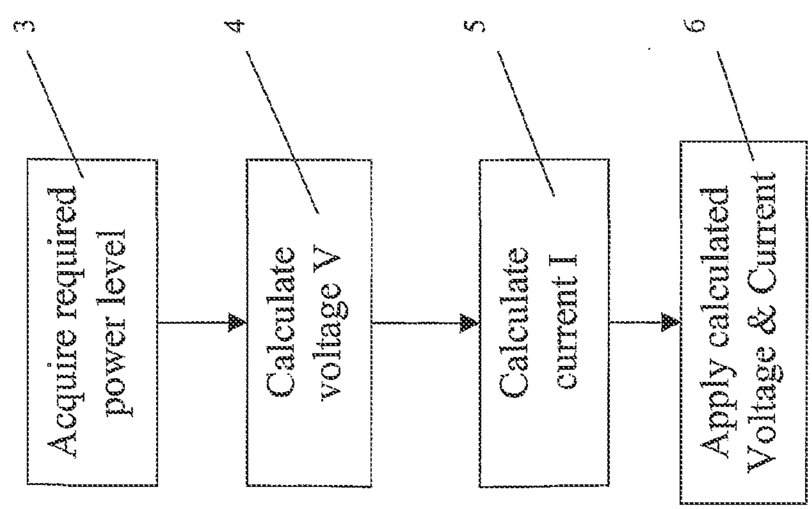


FIGURE 8

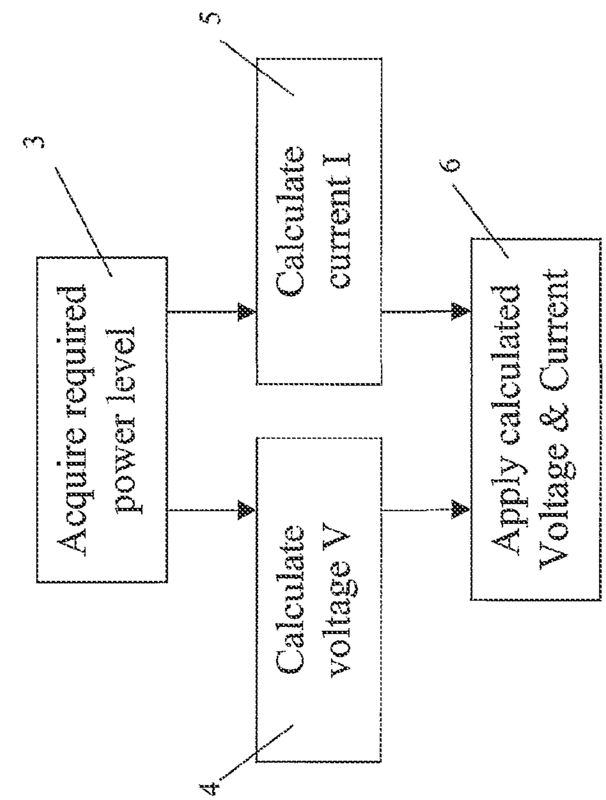


FIGURE 9

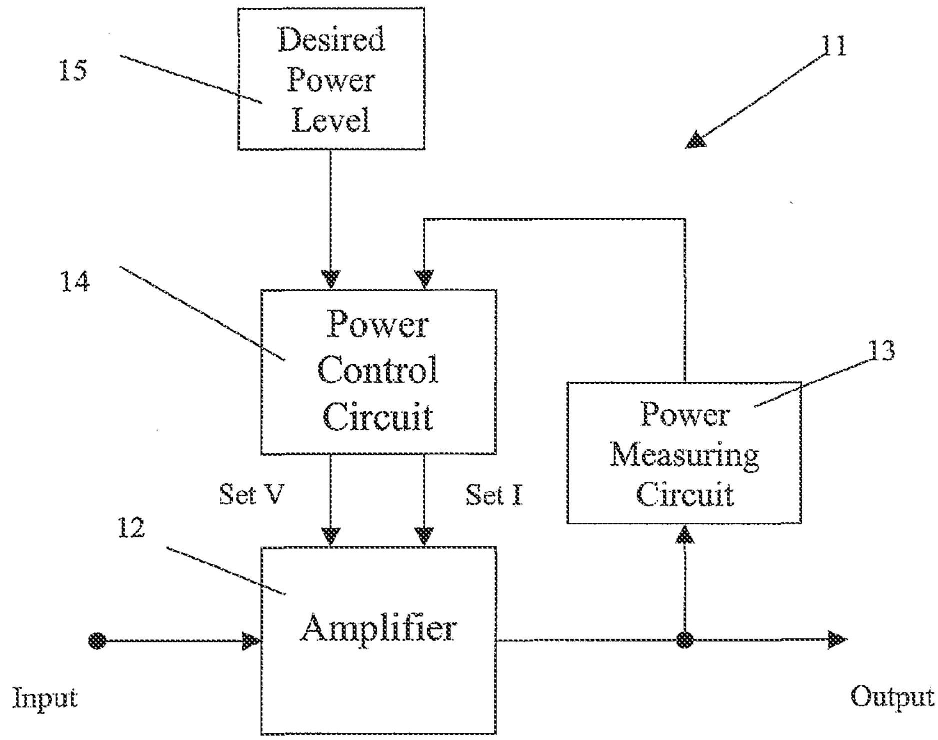

Desired
Power
Level
15
11
14
Power
Control
Circuit
13
Power
Measuring
Circuit
Set V
Set I
12
Amplifier
Input
Output

FIGURE 10

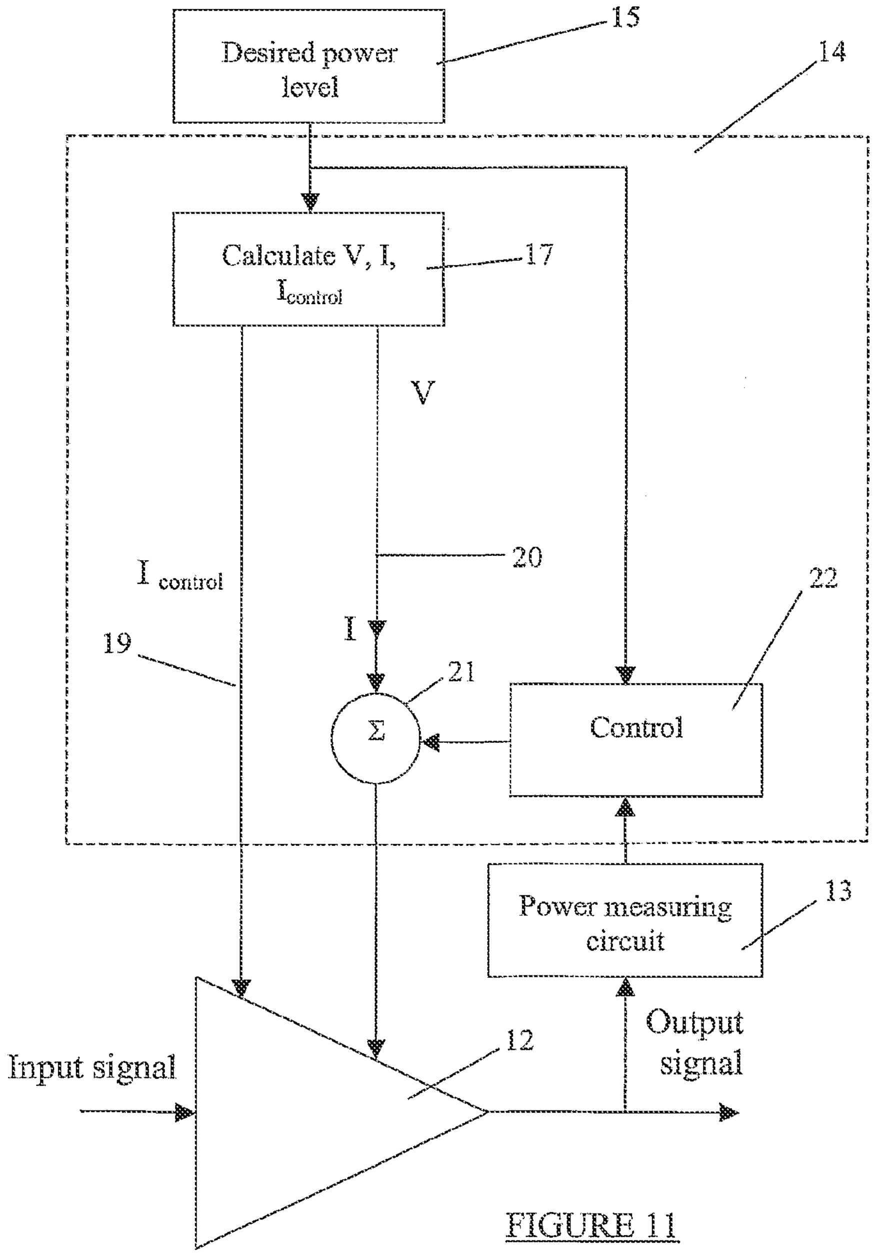

Desired power level
15
14
Calculate V, I, $I_{control}$
17
V
20
22
$I_{control}$
I
19
21
Σ
Control
Power measuring circuit
13
Output signal
12
Input signal

FIGURE 11

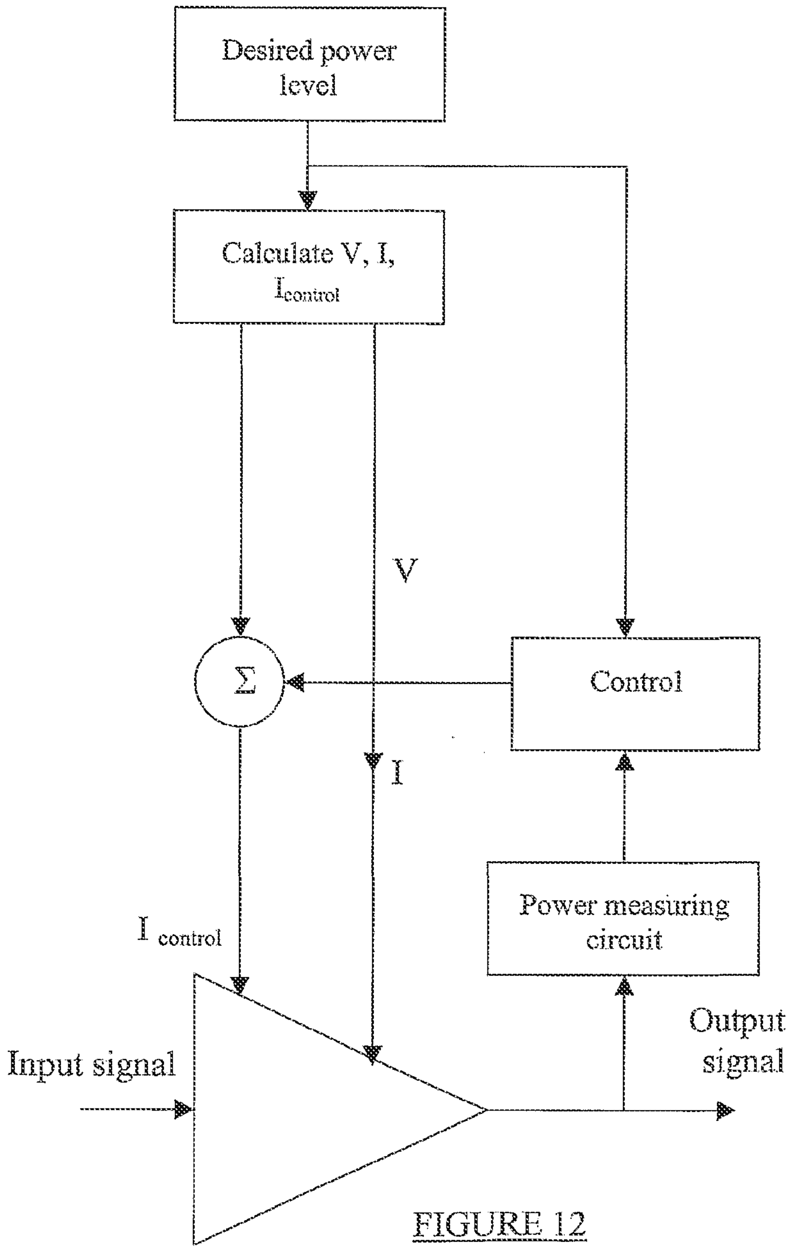

Desired power level
Calculate V, I, $I_{control}$
V
Control
I
$I_{control}$
Power measuring circuit
Output signal
Input signal

FIGURE 12

INTERNATIONAL SEARCH REPORT

PCT/GB 01/05182

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 043 707 A (BUDNIK BRIAN JOSEPH) 28 March 2000 (2000-03-28) column 6, line 3 -column 8, line 9; figures 8,9	1-38
X	GB 2 316 561 A (MOTOROLA LTD) 25 February 1998 (1998-02-25) the whole document	1-38
X	US 5 642 378 A (DENHEYER BRIAN JOHN ET AL) 24 June 1997 (1997-06-24) column 6, line 19 -column 6, line 31; figure 5	1-38
X	GB 2 332 997 A (SAMSUNG ELECTRONICS CO LTD) 7 July 1999 (1999-07-07) page 16, line 5 -page 19, line 24; figure 3	1-38

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2002	25/03/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Fedi, G

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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